

IN THE SPECIFICATION:

1. Please amend the following paragraphs starting on page 10, line 23 as follows:

[FIG. 9] FIG. 9 is a ~~plan~~ planar view showing an example of an arrangement of an infrared sensor array according to the fourth embodiment of the present invention.

[FIG. 10] FIG. 10 is a ~~plan~~ planar view showing an example of an arrangement of an infrared sensor array according to the fourth embodiment of the present invention.

[FIG. 11] FIG. 11 is a ~~plan~~ planar view showing an example of an arrangement of an infrared sensor array according to the fourth embodiment of the present invention.

[FIG. 12] FIG. 12 is a ~~plan~~ planar view showing an example of an arrangement of an infrared sensor array according to the fourth embodiment of the present invention.

2. Please amend the following paragraphs starting on page 11, line 7 as follows:

[FIG. 14] FIG. 14 is a ~~plan~~ planar view showing an example of an arrangement of an infrared sensor array according to the fifth embodiment of the present invention.

[FIG. 15] FIG. 15 is a basic circuit diagram showing an example of charge storage means used in an infrared sensor array according to the ~~fifth~~ sixth embodiment of the present invention.

[FIG. 16] FIG. 16 is a timing diagram showing an operation of charge storage means used in an infrared sensor array according to the ~~fifth~~ sixth embodiment of the present invention.

3. Please amend the following paragraph starting on page 15, line 13 as follows:

[0038] First, at time T1, the voltage of the capacitor element control line 10 is brought to a high ("H") level and the reference capacitor element control switch 5 is turned ON, thereby connecting the reference capacitor element 2 to the series capacitor element 1. Then, at time T2, the voltage of the bias control line 9 is brought to the "H" level, and the bias control switch 4 is turned ON, thereby bringing the voltage of the output node 15 to a bias voltage $[[VB]] \underline{V_B}$.

4. Please amend the following paragraph starting on page 16, line 6 as follows:

[0041] Then, at time T4, the voltage of the signal line 11 is brought to the "H" level and the infrared-detecting capacitor element control switch 6 is turned ON, thereby connecting the infrared-detecting capacitor element 3 to the series capacitor element 1. Then, at time T5, the voltage of the bias control line 9 is brought to the "H" level, thereby bringing the voltage of the output node 15 back to a level equal to the bias voltage $[[VB]] \underline{V_B}$. Then, at time $[[T5]] \underline{T6}$, the voltage of the power supply line 8 is raised from V_L to V_H . Thus, the voltage difference ($V_H - V_L$) between V_H and V_L is distributed according to the capacitance ratio between the series capacitor element 1 and the infrared-detecting capacitor element 3 and added to the voltage of the output node 15. The voltage of the output node 15 in this state is defined as a detection potential V_{sig} .

6. Please amend the following paragraph starting on page 19, line 8 as follows:

[0052] First, at time T0, the voltage of the first vertical scanning line 33 is brought to the "H" level, thereby connecting the infrared sensor 20 and the infrared sensor 21, forming the first row of the infrared sensor array, to the power supply line 8. Then, at time T1, the voltage of the

reference capacitor element control line 10 is brought to "H", thereby connecting the series capacitor element 1 and the reference capacitor element 2 in series with each other. Then, at time T2, the voltage of the bias control line 9 is brought to the "H" level, thereby bringing the voltage of the output node 15 to the bias voltage V_B .

7. Please amend the following paragraph starting on page 19, line 8 as follows:

[0054] Then, the voltage of the power supply line 8 is brought back to V_L and the voltage of the reference capacitor element control line 10 is brought to the "L" level, ~~after which then,~~ the voltage of the infrared-detecting capacitor element control line 11 is raised from V_L to V_H at time T4 ~~brought to the "H" level~~, thereby connecting the series capacitor element 1 and the infrared-detecting capacitor element 3 in series with each other at time T4. Then, the voltage of the bias control line 9 is brought to the "H" level at time T5, thereby bringing the voltage of the output node 15 back to the bias voltage V_B .